Managing Device Variations in Microprocessors

2002 Designing Robust Circuits and Systems with Unreliable Components Workshop

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Managing Device Variation Overview

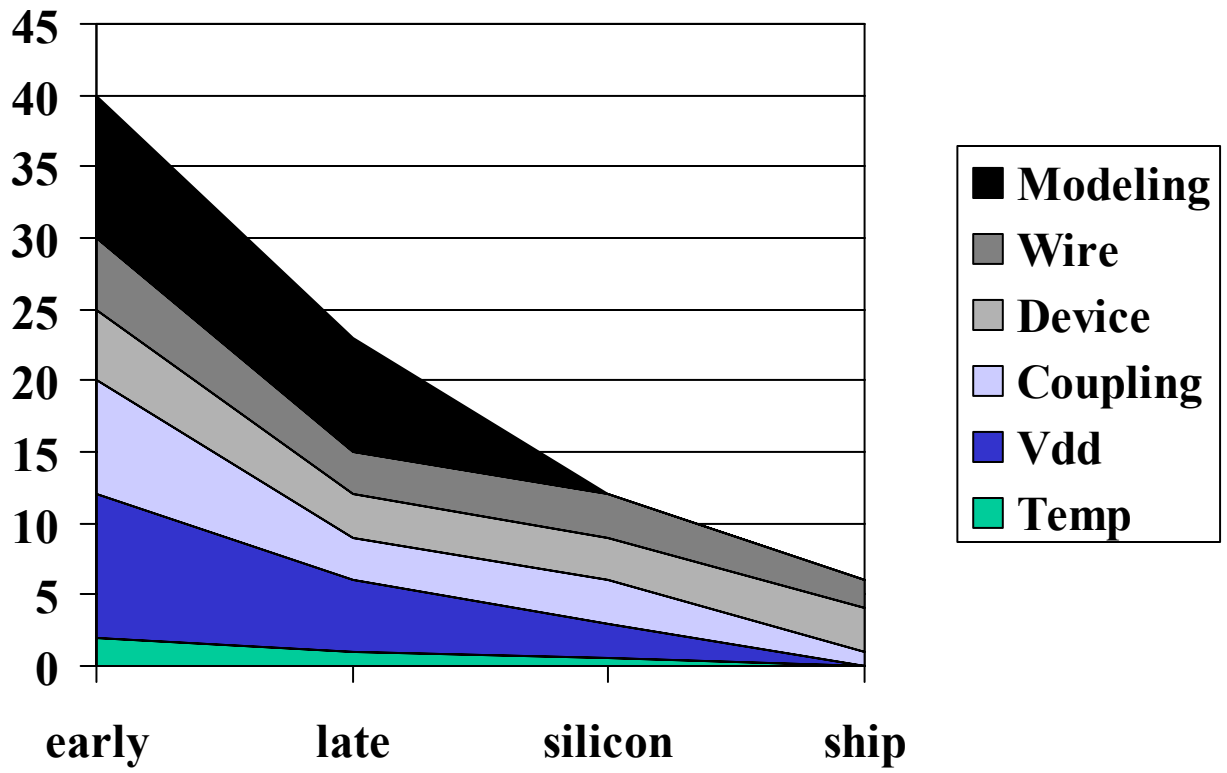
- My perspective: synchronous, digital design where **performance/power** is the optimization point
- My goal: to understand the variations over which we have *some control* from a design perspective
  - How to analyze the variations
  - How to incorporate such information into *tools* and *methodologies* with a maximum ROI
  - Adaptive approaches for minimizing the impact of variation on critical performance metrics

Sources of Variation

- Environmental & Modeling
  - Changes in Vdd, Temperature and coupling (capacitive and inductive)
  - Tool and modeling inaccuracy
- Manufacturing
  - Random
    - RDF for Vt variations, ΔL, Metal etch etc.
  - Systematic
    - Mask generation algorithms, layout induced impacts, wearout mechanisms

Sources of Variation

- What can be analyzed (variability) vs. what cannot (uncertainty) changes as the design progresses
- Total variation never completely disappears

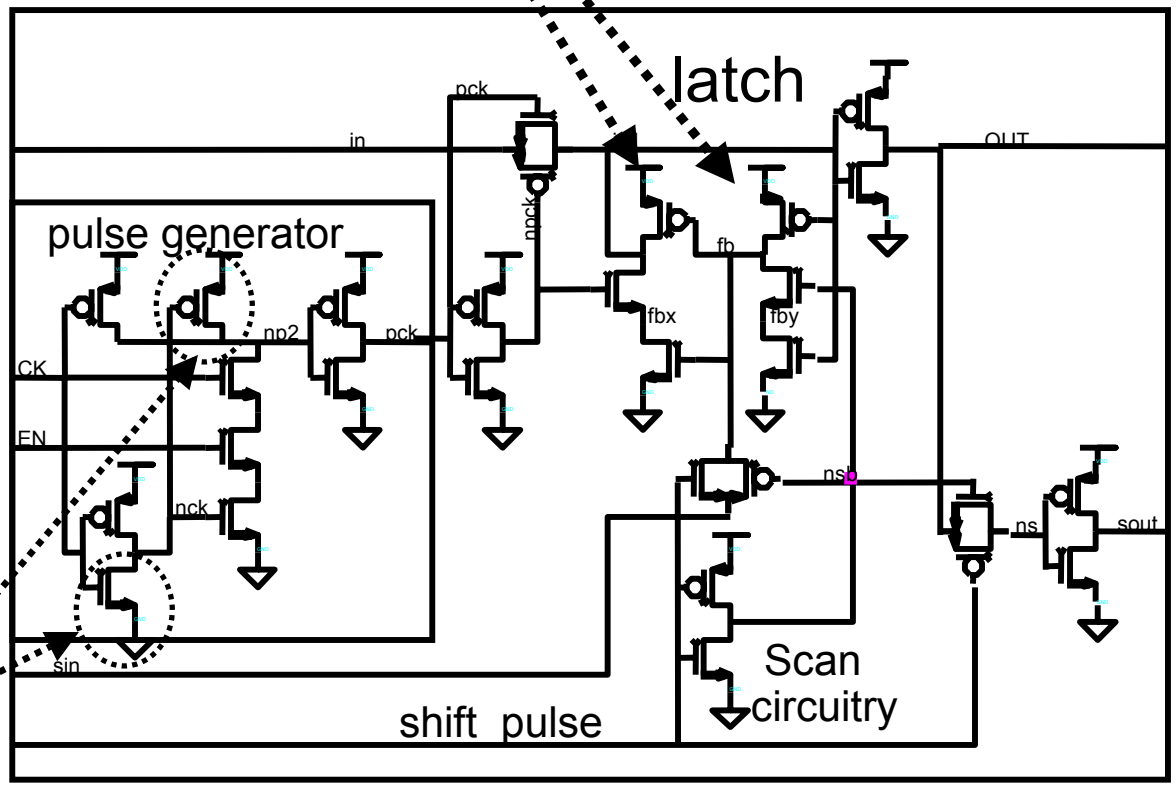


Variation Impacts on Processors

- Sensitive circuit behavior
  - Margin for pulse generators and other self-timed circuits
  - Drive fights for jam latches and pseudo-NMOS, precharge and charge sharing for domino
  - PLLs and I/O drivers
    - Stability, impedance and slew matching
- Path delays
  - Clock distribution skew
  - Min and max time path delay changes

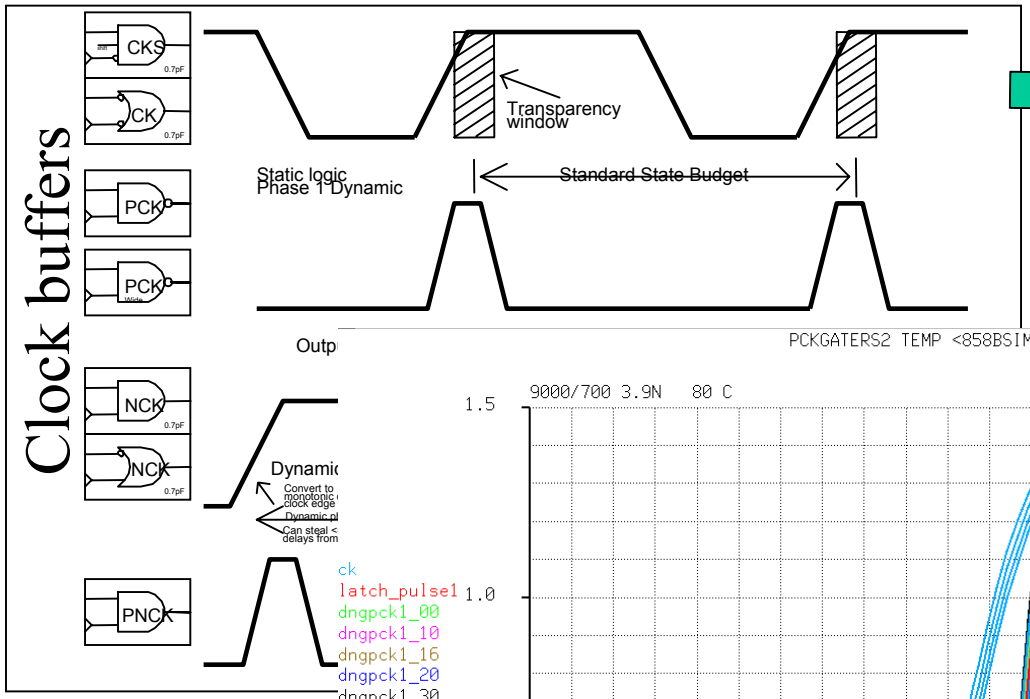
Variation Impacts on Circuits

Drive fights against these transistors ➔ variations endanger the setting of the latch

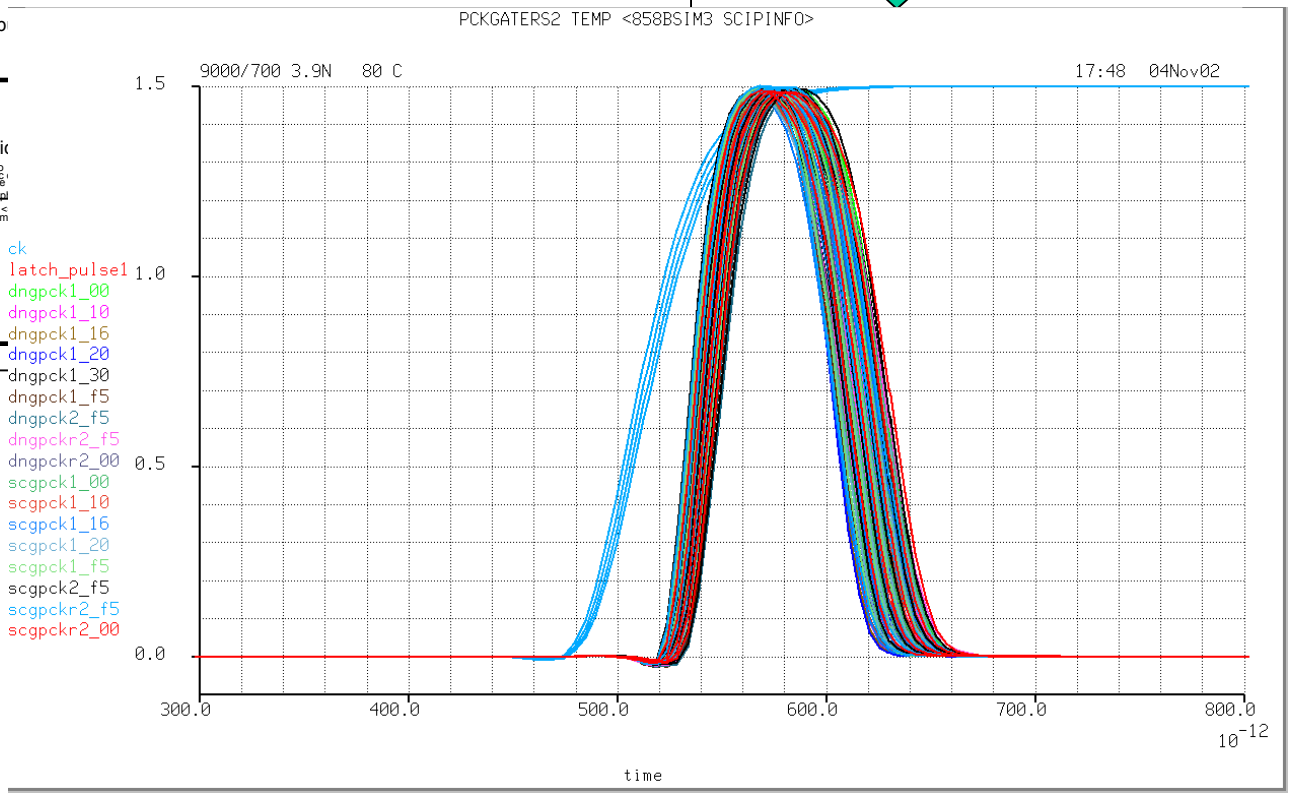


Key Transistors for pulse width management. Variations create set margin and hold time issues

Clock Waveforms With Variations



Actual McKinley logical and physical clocks



Tool Changes for Dealing with Variation

- Statistical incorporation of *random variations*
  - Used for some time in SPICE modeling to deal with device variations
    - Results in the necessary design margin values
  - Timing models for path length dependent variation, and arrival time distributions
    - Can apply more margin to paths with greater variability – both min and max time
  - Electrical checks such as coupling noise
    - Probability of alignment of supply offsets, charge sharing, worst case data patterns etc. can be estimated and included in margins

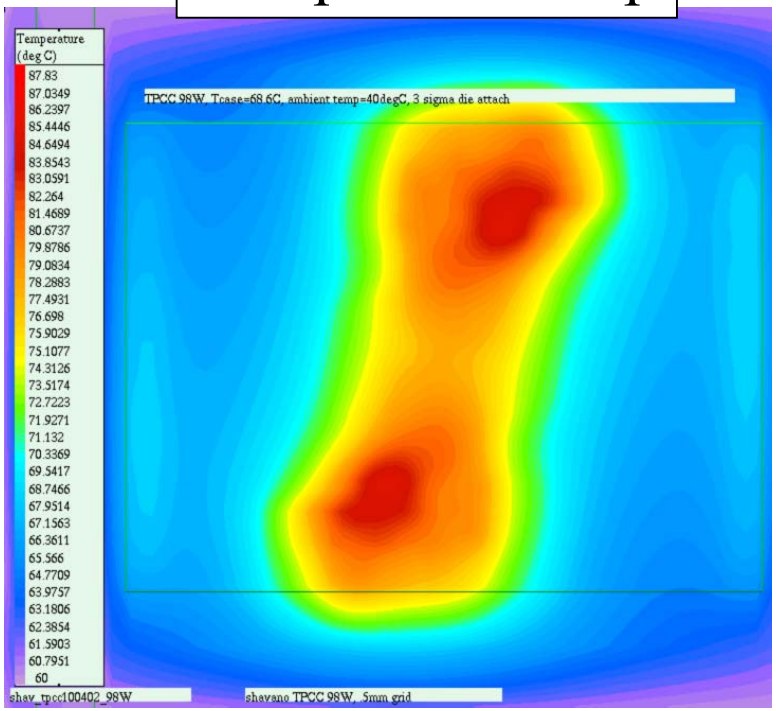
Tool Changes for Dealing with Variation

- Incorporation of *known variation* in modeling
  - Timing analysis can include progressively more information about local supplies, temperature and path length as the design matures
    - Channel design effort towards the areas that are *most likely* to produce issues in silicon
  - Electrical quality checks can incorporate environmental information for significant effort reduction
    - Electromigration / self-heating, coupling noise etc.

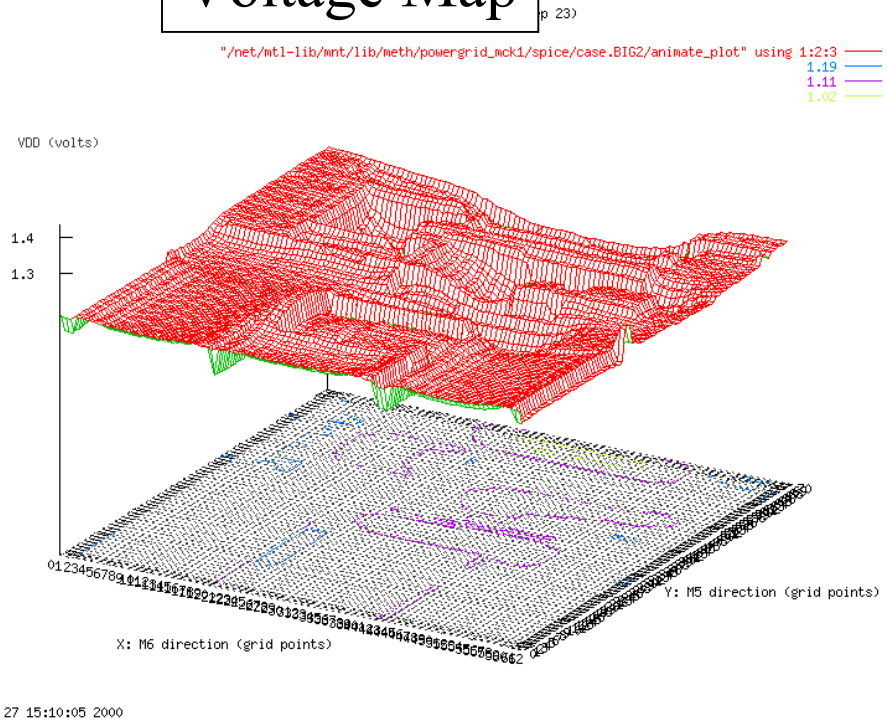
Tool Changes for Dealing with Variation

- Incorporation of *known variation* in modeling
  - Example sources of data

Temperature Map



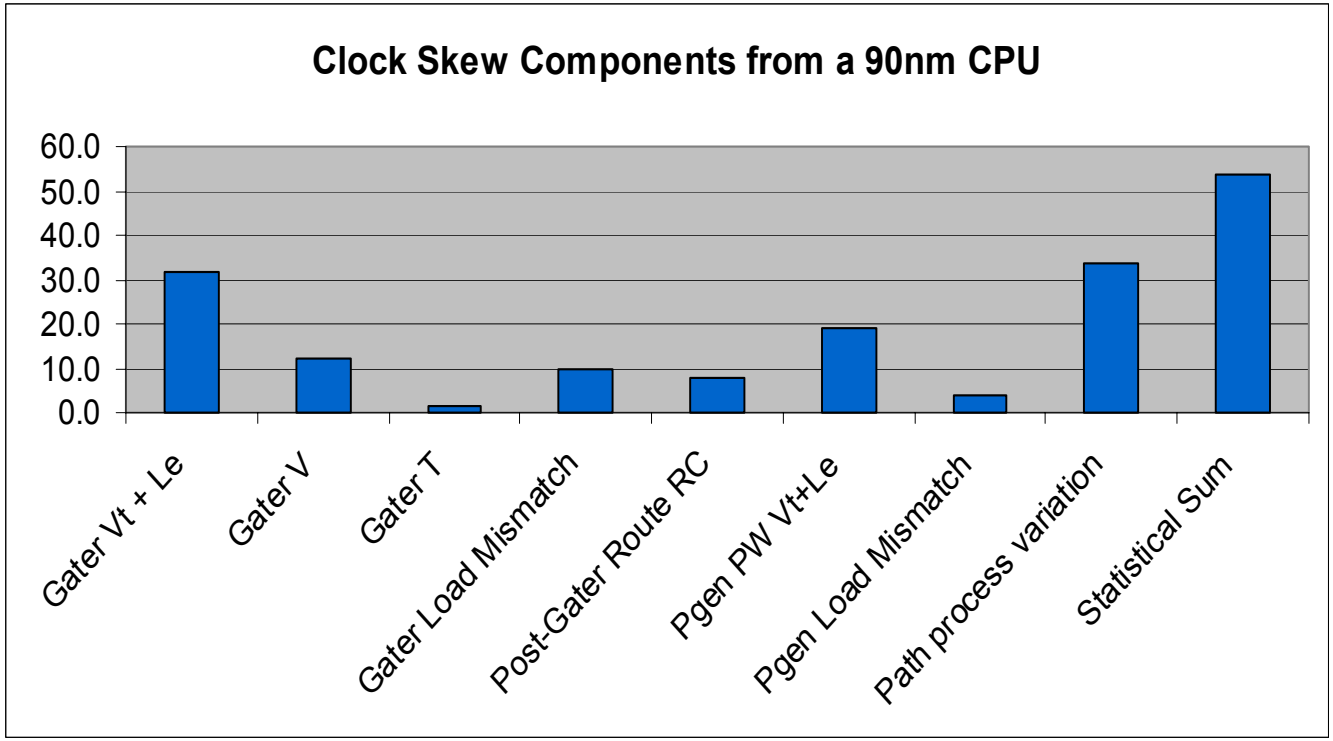
Voltage Map



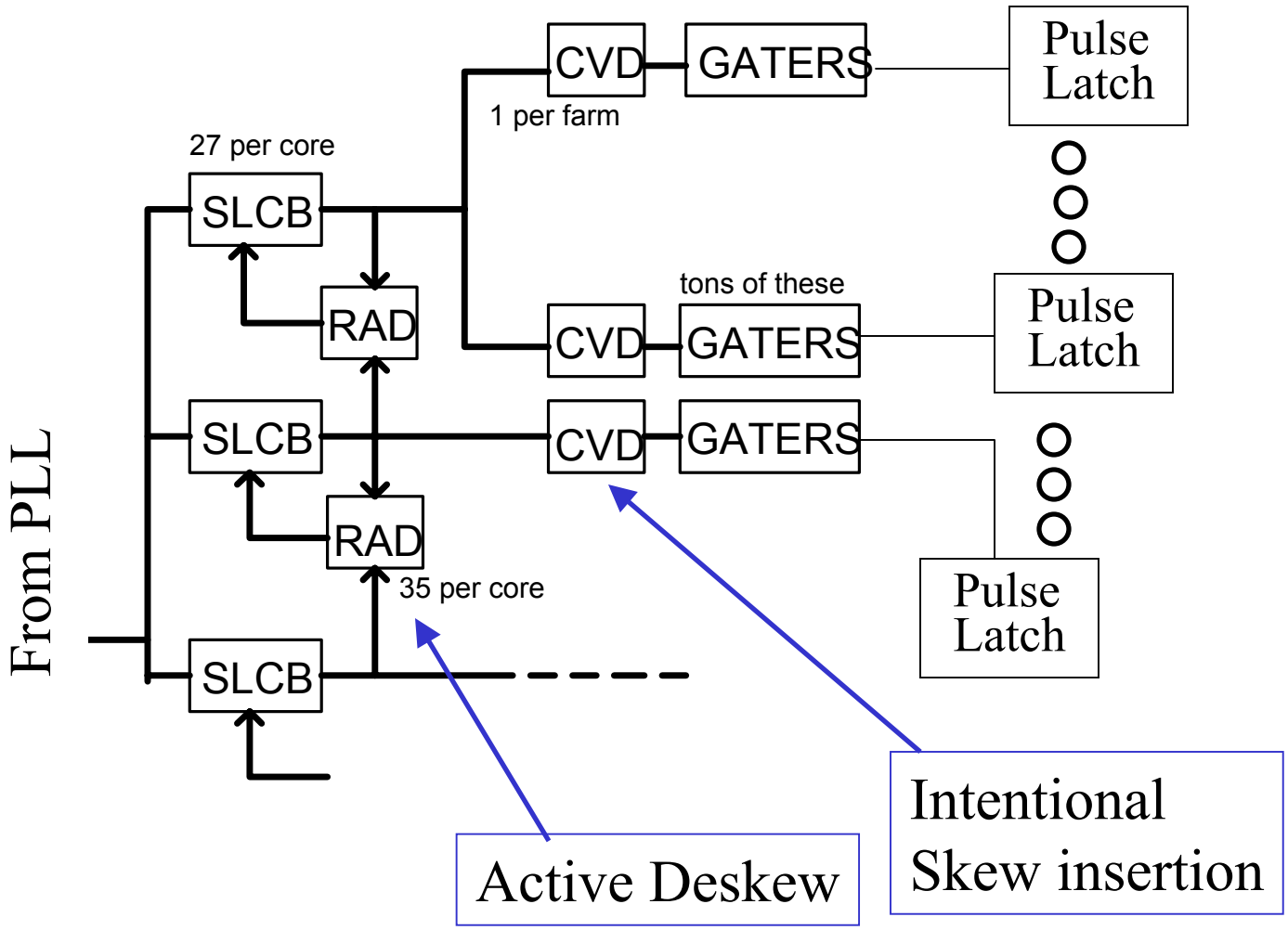
Design Methodologies for Dealing with Variation

- Analysis of sensitive circuits ➔ e.g. clocks
  - Do a 5σ analysis of individual circuits and use monte-carlo simulations to find the sum

- Variation can be reduced with long L devices, careful layout, & circuit topologies formerly in the analog domain



Clock Distribution Block Diagram



Design Methodologies for Dealing with Variation

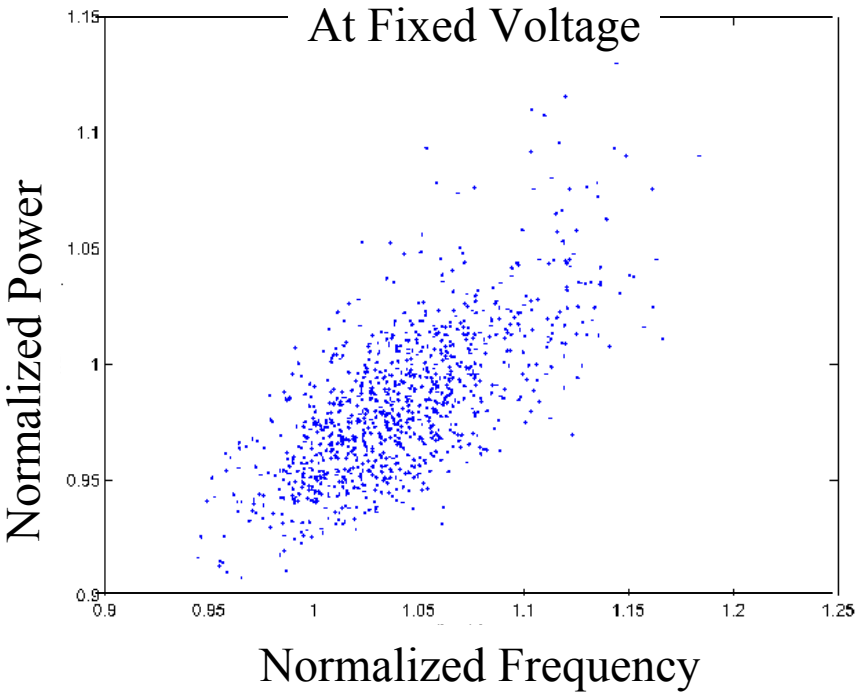
- Example: Management of clock skew
  - Most obvious and significant impact of variation
- Every year at ISSCC there are several papers on clock distribution and skew management
  - Distribution design and analysis techniques to reduce know variations to a negligible level
  - Active deskew schemes involving phase comparators and delay lines, tuned clock sources etc.
  - Skew tolerance methods involving cycle stealing latches, hold time margin etc.
- In addition to skew elimination, active clock control is desired ➔ insert *intentional* skew where it helps
  - Duty cycle control can provide another important knob

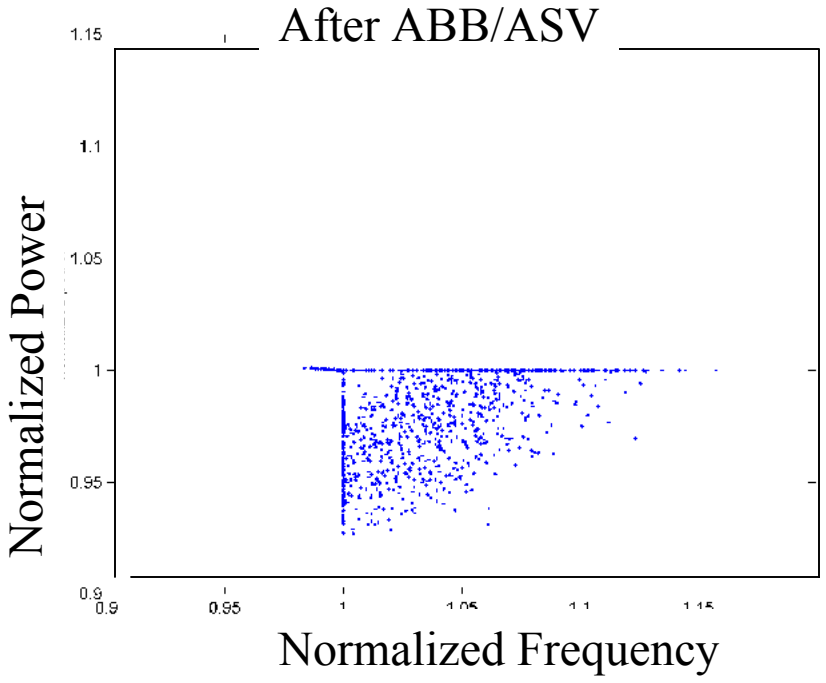
Adaptive Approaches for Dealing with Variation

- Once circuits have been designed with sufficient margin to *function properly* in the face of large variations, the next issue is *optimizing* power and performance
- ➢ I call this *adaptive silicon*
- I already discussed methods for adapting clock arrivals to variable conditions
- Other means of adapting to variation that are being explored are Adaptive Body Bias (ABB) and Adaptive Supply Voltage (ASV)

Adaptive Approaches for Dealing with Variation

- Adaptive Body Bias (ABB) and Adaptive Supply Voltage (ASV)

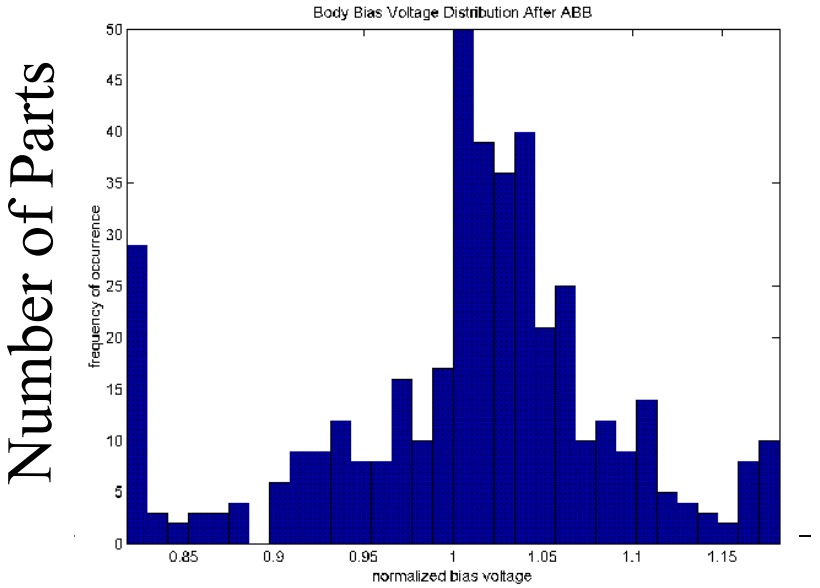




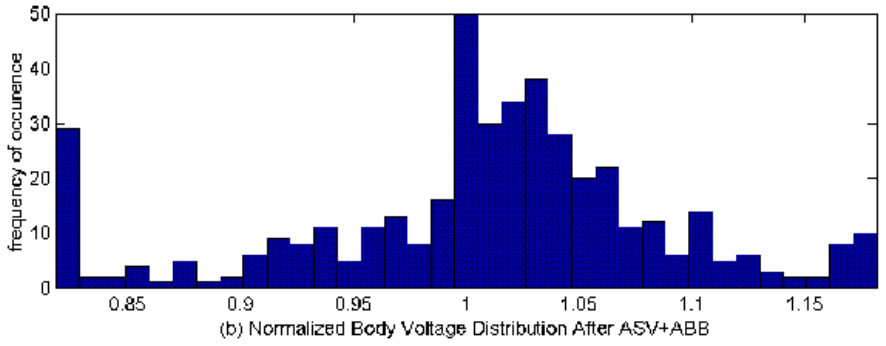
Adaptive Approaches for Dealing with Variation

- Adaptive Body Bias (ABB) and Adaptive Supply Voltage (ASV)

ABB Results



ASV



Adaptive Approaches for Dealing with Variation

- Algorithmic optimization of tuning knobs via scan control per-part at manufacturing test
  - With clock skew, body bias and supply voltage all dynamically controllable, optimal settings per-part can be determined empirically
  - Part-part variation can be dramatically reduced which results in improved average power / performance
  - Parallel search optimizations can be used such as genetic algorithms
- Control capability can be increased in granularity as intra-die variation comes to dominate
  - Local clocks, multiple supply and body voltage domains per-chip etc.

Conclusion

- Processor designers will be spending more and more effort on variation issues
  - Moving factors from the “random” bin to the “systematic” bin
  - Statistical factors included in analysis tools
  - Incorporating increasing numbers of tuning capabilities for post-design silicon optimization
- Nothing that a larger design team can’t handle ☺